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Code No: A0602, A5502, A5702

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March/April 2011

VLSI TECHNOLOGY AND DESIGN

(COMMON TO DIGITAL SYSTEM AND COMPUTER ELECTRONICS, EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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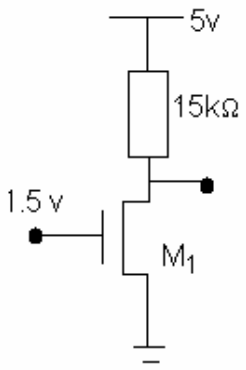
1.a) Explain the process of fabrication for CMOS technology with neat diagrams.
b) Compare B_iCMOS technology with other Technologies. [6+6]

2.a) Calculate I_D and V_{DS} if k_n = 100 µA/v^2, V_{tn} = 0.6v and W/L =3 for transistor M, in the circuit in shown in figure.



b) Determine the pull up to pull down ratio for an nMOS inverter driven by another inverter. [6+6]

3.a) Write the design rules for contact cuts.
b) What are the limitations for scaling?
c) What are the various construction rules for transistors? [12]

4.a) What are the advantages of pseudo – nMOS logic? Draw the circuit diagram of pseudo – nMOS NOR fate and explain its operation.
b) Draw the model for derivation of delay unit and derive its value for 5 µm technology. [6+6]

5.a) What is barrel shifter? How to use it in VLSI design?
b) How to list a combinational logic networks? Give some simulation tools. [6+6]

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6.a) Draw a circuit diagram for 4 – transistor SRAM cell and explain how it stores data?
b) Write short notes on the clocking discipline for sequential systems. [6+6]

7.a) What is mean by floor planning? Explain the different methods of floor planning.
b) Design a circuit for input pad connectivity and explain its necessity in chip design. [6+6]

8.a) Explain the various Architectures to reduce the power.
b) Explain how scheduling determines time cost. [6+6]

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